REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Official Action dated May 11, 2005. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 1-20 are under consideration in this application. Claims 1-3 and 7 are being amended, as set forth above, in order to more particularly define and distinctly claim Applicants' invention.

The claims are being amended to correct formal errors and/or to better disclose or describe the features of the present invention as claimed. Applicants hereby submit that no new matter is being introduced into the application through the submission of this response. In particular, the amendment to claim 3, "manufactured LSI" for verification is shown as "REAL LSI" at the right lower corner of Fig. 2 and described on page 23, last paragraph.

Formality Rejection

Claim 3 was rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. As indicated, the claim is being amended as required by the Examiner. Accordingly, the withdrawal of the outstanding informality rejection is in order, and is therefore respectfully solicited.

Prior Art Rejections

Claims 1-15 and 18-19 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,446,243 to Huang et al. (hereinafter "Huang"), and claims 16-17 and 20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Huang in view of U.S. Patent No. 6,782,511 to Frank et al. (hereinafter "Frank"). The references of Dey (6,687,710), Dole (6,634,008), Watanabe et al. (6,157,947), Ara et al. (6,654,935), Rostoker et al. (5,867,399), Lee et al. (6,102,961), and Nakagawa (JP2002024311) were cited as pertinent to

the application. These rejections have been carefully considered, but are most respectfully traversed.

The system verification method to be applied by an intellectual property user for verifying operation of an integrated system design constructed with modules designed in-house and at least one module protected as intellectual property of an outside entity of the invention, as recited in claim 1, comprises: providing design data or a verification model of each of the modules; simulating the operation of the integrated system with one of the input vector sequences so as to obtain a respective output vector sequence. The simulating step includes the steps of: dividing a simulation time period into a finite number of time steps in sequence from time 0 to time n; supplying an input vector for said each of the modules at one time step, while observing an internal state of said each module at the respective time step; computing an output vector from said each in-house designed module and the internal state at a starting time of a time step subsequent to the time step, based on the design data or the verification model; transmitting an input vector for said each module of the outside entity to the outside entity at said one time step through a communication line (e.g., an exchange communication line, the Internet, or exclusive line, as in the Fig. 1) such that the outside entity simulates operation of said each module with the input vector at said one time step so as to compute an output vector; receiving the output vector from the outside entity through a communication line at a beginning of the subsequent time step; integrating the output vectors from all modules at the subsequent time step to obtain an output of the whole system at the subsequent time step; and repeating the supplying, computing, transmitting, receiving and integrating steps from time 0 to time n sequentially to obtain an output sequence of the whole system.

Claim 2 recites a system verification equipment implementing the method recited in claim 1.

The invention as recited in claim 7 is directed to a system verification equipment to be applied by an intellectual property provider for verifying operation of at least one module protected as intellectual property and included in an integrated system design in conjunction with modules designed in-house by an integrated system designer, said equipment comprising: storage medium for storing design data or a verification model of said module; receiving means for receiving an input vector sequence from the integrated system designer at one time step through a communication line; simulating means for simulating the operation of the module with the input vector sequence so as to obtain a respective output vector

sequence; and sending means for sending the output vector sequence to the integrated system designer through a communication line at a beginning of the subsequent time step. The time step and the subsequent time step are defined and supplied by the integrated system designer.

Applicants respectfully contended that Huang fails to teach or suggest (1) such "a system verification method to be applied by an intellectual property user including (i) transmitting an input vector for said each module of the outside entity to the outside entity at said one time step through a communication line *such that the outside entity simulates operation of said each module with the input vector at said one time step* so as to compute an output vector, and (ii) receiving the output vector from the outside entity through a communication line at a beginning of the subsequent time step"; or (2) such "a system verification equipment to be applied by an intellectual property provider including (1) receiving means for receiving an input vector sequence from the integrated system designer at one time step through a communication line, and (ii) sending means for sending the output vector sequence to the integrated system designer through a communication line at a beginning of the subsequent time step" according to the invention.

In contrast, Huang's system verification method for verifying the operation of system by physically incorporating the IP provider's design modules (Figs. 4-6) that are protected as intellectual property (col. 3, line 21; col. 4, line 33) into the system of the IP user, as a verification module therein(col. 4, lines 38-42; Fig. 2). Huang does not provide any communication line which transfers input or output vector between the IP user and the IP provider for target system verification. By using such a communication line of the invention, the IP *service* provider can provide IP verification services without providing the IP verification model/program itself, and this leads to high level security of IP (p. 27, lines 8-15).

Applicants respectfully contend that one skilled in the art would not be motivated to provided any communication line into Huang's system verification as the IP provider's design modules are physically incorporated therein. Even if, arguendo, one skilled in the art connected a communication line between The IP provider's verification module with components in Huang's system, such combined teachings would still fall short in fully meeting the Applicants' claimed invention as set forth in independent claims since, as discussed, there is no teaching of "the outside entity simulates operation of said each module with the input vector at said one time step so as to compute an output vector" in either Huang.

Frank was relied upon by the Examiner to cover the features recited in claims 16-17

and 20. however, Frank only discloses a pay-per-use application server provide downloadable modules to IP user (col. 1, line 67- col. 2, line 7), rather than "the outside entity simulates operation of said each module with the input vector at said one time step so as to compute an output vector" without providing the verification program itself (i.e., not downloable by an IP user).

As such, Frank also does not charge simulation services performed by the outside IP owner by quantity of load on the simulating server of the IP owner (claim 16), or by the quantity of input vector data transmitted to the IP owner's server (claim 17).

Applicants contend that cited prior art references or their combination fails to teach or disclose each and every feature of the present invention as recited in independent claims 1-2 and 7. As such, the present invention as now claimed is distinguishable and thereby allowable over the rejections raised in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

Conclusion

In view of all the above, Applicants respectfully submit that certain clear and distinct differences as discussed exist between the present invention as now claimed and the prior art references upon which the rejections in the Office Action rely. These differences are more than sufficient that the present invention as now claimed would not have been anticipated nor rendered obvious given the prior art. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application as amended is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to

contact the Applicant's undersigned representative at the address and phone number indicated below.

Respectfully submitted,

Stanley P. Fisher
Registration Number 24,344

Juan Carlos A. Marquez
Registration Number 34,072

REED SMITH LLP
3110 Fairview Park Drive, Suite 1400
Falls Church, Virginia 22042
(703) 641-4200

September 12, 2005

SPF/JCM/JT